

# JS120KQ

Rev.0.1 Oct.17 2024

## Description

- 1) A package consists of two inverse parallel SCR chips, which rated voltage is up to 1800V
- 2) Welding by vacuum welding technology, which provide high reliability
- 3) Insulated by silicone gel, provide a insulation voltage of 3000V~
- 4) UL 1557 item recognized. (File No.: E252906)

## Typical Application

Soft start, solid state relay, AC/DC switch, temperature control.

## Absolute Maximum Ratings (Packaged into modules, unless otherwise specified, $T_{CASE}=25^{\circ}\text{C}$ )

Parameter	Test Conditions	Symbol	Values	Unit
Operating junction temperature range		$T_J$	-40-125	°C
Repetitive peak off-state voltage	$T_J=25^{\circ}\text{C}$	$V_{DRM}$	1200/1600/1800	V
Repetitive peak reverse voltage	$T_J=25^{\circ}\text{C}$	$V_{RRM}$	1200/1600/1800	V
RMS on-state current	$T_C=80^{\circ}\text{C}$	$I_{T(RMS)}$	135	A
Peak on-state surge current	$t_P=10\text{ms} V_R=0.6V_{RRM}$	$I_{TSM}$	2000	A
$I^2t$ value for fusing	$t_P=10\text{ms} V_R=0.6V_{RRM}$	$I^2t$	20000	$\text{A}^2\text{s}$
Critical rate of rise of on-state current	$I_G=2 \times I_{GT}$	$di/dt$	150	$\text{A}/\mu\text{s}$

## Electrical Characteristics (Packaged into modules, unless otherwise specified, $T_{CASE}=25^{\circ}\text{C}$ )

Parameter	Test Conditions	Symbol	Values	Unit
Peak on-state voltage	$I_T=300\text{A} t_P=380\mu\text{s}$	$V_{TM}$	$\leq 1.85$	V
Threshold voltage	$T_J=125^{\circ}\text{C}$	$V_{TO}$	$\leq 0.9$	V
Dynamic resistance	$T_J=125^{\circ}\text{C}$	$R_d$	$\leq 3.5$	$\text{m}\Omega$
Repetitive peak off-state current	$V_D=V_{RRM}$ $T_c=25^{\circ}\text{C}$ $T_c=125^{\circ}\text{C}$	$I_{DRM1}$ $I_{DRM2}$	$\leq 100$ $\leq 20$	$\mu\text{A}$ mA
Repetitive peak reverse current	$V_R=V_{RRM}$ $T_c=25^{\circ}\text{C}$ $T_c=125^{\circ}\text{C}$	$I_{RRM1}$ $I_{RRM2}$	$\leq 100$ $\leq 20$	$\mu\text{A}$ mA
Triggering gate current	$V_D=12\text{V} R_L=30\Omega$	$I_{GT}$	20-120	mA
Holding current	$I_T=1\text{A}$	$I_H$	$\leq 250$	mA

Latching current	$I_G=1.2I_{GT}$	$I_L$	$\leq 350$	mA
Triggering gate voltage	$V_D=12V R_L=30\Omega$	$V_{GT}$	$\leq 1.5$	V
Non triggering gate voltage	$V_D=V_{DRM} T_J=125^\circ C$	$V_{GD}$	$\geq 0.2$	V
Critical rate of rise of voltage	$V_D=2/3V_{DRM} T_J=125^\circ C$ Gate Open	$dv/dt$	$\geq 1000$	V/ $\mu$ s
Thermal resistance	Junction to case	$R_{th(j-c)}$	0.45	°C/W

### Mechanical Characteristics

Module size	40.5×28mm
Module height	15.48mm
 	symbol

### Ordering Information

JS

120

KQ

-12

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 $I_{T(RMS)}=135A$ 

12: $V_{DRM}/V_{RRM} \geq 1200V$   
16: $V_{DRM}/V_{RRM} \geq 1600V$   
18: $V_{DRM}/V_{RRM} \geq 1800V$ 

Module of anti-parallel of SCRs